(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 049 309 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
02.11.2000 Bulletin 2000/44

(51) Int. Cl.[7]: **H04L 29/12**, H04L 12/28

(21) Application number: **00108805.3**

(22) Date of filing: **26.04.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **29.04.1999 US 304212**

(71) Applicant:
MITSUBISHI DENKI KABUSHIKI KAISHA
Tokyo 100-8310 (JP)

(72) Inventors:
- **Akatsu, Shinji**
  2 chome, Chiyoda-Ku, Tokyo100-8310 (JP)
- **Matsubara, Fernando-Masami**
  Apt: 201 Santa Carla, CA 95054 (US)
- **Miura, Shin**
  2-chome, Chiyoda-ku, Tokyo 100-8310 (JP)

(74) Representative:
Pfenning, Meinig & Partner
Mozartstrasse 17
80336 München (DE)

(54) Address mapping

(57) A method for address mapping in a home entertainment network system includes receiving a self identification packet; extracting a bus identifier and a physical identifier from the self identification packet; adding a new row to an address mapping table, the new row comprising a bus identifier field, a physical identifier field, and a node unique identifier field; inserting the physical identifier and bus identifier into the respective bus identifier and physical identifier field in the new row of the address mapping table; transmitting a read request packet to a node identified by the self identification packet; receiving a read response packet, the read response packet comprising a node unique identifier; extracting one or more identifiers from the read response packet, the one or more identifiers including a node unique identifier; and inserting the one or more identifiers into additional fields in the new row of the address mapping table.

EP 1 049 309 A2

Description

BACKGROUND OF THE INVENTION

Cross Reference to Related Applications

[0001] This application is related to U.S. application Ser. No. 09/140,899, filed August 25, 1998, entitled "BITMAP TRANSFER IN PLUG AND PLAY NETWORK", U.S. application Ser. No. 09/144,678, filed August 31, 1999, entitled "HOME DIGITAL NETWORK INTERFACE", and U.S. application Ser. Nos. [Not Yet Assigned] (attorney docket 235/124), entitled "HOME GATEWAY", [Not Yet Assigned] (attorney docket 235/126), entitled "REMOTE MONITORING AND CONTROL", [Not Yet Assigned] (attorney docket 235/127), entitled "GEOGRAPHIC DATA COLLECTION", [Not Yet Assigned] (attorney docket 235/128), entitled "COMMAND AND CONTROL TRANSFER", and [Not Yet Assigned] (attorney docket 236/259), entitled "BITMAP TRANSFER", all filed on the same day herewith, and all of which are incorporated herein by reference in their entirety.

Field of the Invention

[0002] The present invention pertains generally to the field of home entertainment systems and more specifically to communication and control technologies in home entertainment systems.

Background

[0003] In the past, a home entertainment system frequently consisted of simply a television set (TV) and a video cassette recorder (VCR). One or two coaxial or composite cables interconnected the TV and VCR from input-to-output and/or output-to-input respectively. However, in recent years, home entertainment systems have become increasingly complex.

[0004] Advances in home electronic devices, such as the compact disk (CD) player, digital-video disc (DVD) player, gaming systems, surround sound audio systems, hand held video cameras, etc., naturally compelled consumers to connect the additional devices to their home entertainment system. Each new device added at least two more wires (generally, power and input/output) to the complex web of wires snaking their way in and out of the various devices.

[0005] Originally, switch boxes were employed to cut down on the complexity of the interconnections between the various devices. For example, a simple "A/B" switch box allowed a user to selectively choose one input or another, without having to disconnect and re-engage coaxial cables between the devices. As the number of devices in home entertainment systems increased, however, the use of A/B switch boxes to interconnect the devices becomes cumbersome and inefficient.

[0006] Notably, consumers generally desire less wires, simpler interconnect schemes and, as the functionality and sophistication of home entertainment devices increase, to dispose of the myriad individual component remote controls needed to operate the respective devices. Indeed, most remote control "features" are never used (see. e.g., "The Complexity Problem: Industrial Design", Atlantic Monthly, Vol. 271, No. 3, March 1993, p. 96); if for no other reason, this is due to the differing sequences and/or number of steps involved with the control and operation of each respective device.

[0007] One solution to the aforementioned control problem is proposed in U.S. Patent 5,675,390 (the "390 patent") by Schindler et al. As depicted in FIG. 1 of the '390 patent, an entertainment system is centrally controlled by a personal computer. According to the Schindler et al. system, control is consolidated in the personal computer, wherein a "hub and spoke", or "star" type communication topology is employed — i.e., with all communications passing through the personal computer (or hub). By this configuration, each device requires its own dedicated connection to the personal computer. Such a solution may work well for tightly integrated home electronics equipment and a sophisticated computer user. However, it requires an even greater number of interconnecting wires than were previously employed. (Note the number of I/O plugs depicted in FIG. 7 of the '390 patent). Further, such a system is not scalable. That is, as new devices are to be added to the system, additional corresponding adapters/controllers must be added to the personal computer.

[0008] A similar solution is proposed in U.S. Patent 5,722,041 (the "'041 patent") by Freadman. FIG. 2 of the '041 patent best depicts Freadman's home entertainment system. Like Schindler et al., control is centrally located in a personal computer. Media feeds are through a combination multi-channel modem and analog radio frequency mixer, which connects to a number of terminal devices through a coaxial cable. Although a reduction in the number of wires is accomplished, shared functionality between the devices is minimal, e.g., one device doesn't control another device and vice-versa.

[0009] In particular, adding a user-operated personal computer to control a home entertainment system network does not, in itself, reduce complexity. In fact, it may increase the complexity. The computer is often difficult, if not cum-

bersome to control. Hardware and software components generally need to be configured to communicate, and the devices properly initialized. Upgrades to either peripheral devices (e.g., VCRs, TVs, etc.) or the computer itself may necessitate a complete overhaul of the system operating software, thereby introducing incompatibilities and uncertainties in the system performance.

[0010] With regard to the myriad interconnection wires in more complex home entertainment systems, one solution is the IEEE 1394-1995 standard and its extensions IEEE 1394a, and IEEE 1394b, which are referred to herein as "IEEE 1394". In one embodiment, a IEEE 1394 cable is a six strand cable: one strand for power, one strand for ground, two strands for data, and two strands for strobes used to synchronize the data strands. In an alternative embodiment, a four strand cable can be used, omitting the power and ground strands. IEEE 1394 cable also comprises a shield, which prevents electromagnetic interference. At its core, IEEE 1394 cable is essentially a high performance serial bus, having data rates as of this present writing of up to 400 megabits per second.

[0011] Advantageously, the IEEE 1394 bus reduces the need for the myriad wires in a home entertainment system, as the component electronic devices may be designed to receive power and communication through the IEEE 1394 cable, thereby reducing the connections needed for most devices to as few as a single cable in a backplane bus environment. The IEEE 1394-1995 standard provides a specification for aspects of the physical, link and transaction layers for implementing of the IEEE 1394 bus, including provisions for such functions as resetting the bus, bus arbitration, node configuration, standard packet structures, initializing packet transmission, sending and receiving asynchronous packets, sending and receiving isochronous packets, transaction control, and error detection and correction.

[0012] Communication over IEEE 1394 bus differs from many previous technologies in that it is purely digital. In particular, data carried on the IEEE 1394 bus is either digital from the source (e.g., a CD-ROM), or it must be converted by an analog-to-digital converter before being placed on the IEEE 1394 bus. Further, communication in a IEEE 1394-based system is peer-to-peer, i.e., each device (a.k.a. "node") on the IEEE 1394 bus can communicate with any other node without requiring communication/control requests to be processed through a central device/node (e.g., as is required in a "client-server" type configuration). In a IEEE 1394-based system, the controller can reside in any node, so in a sense, the IEEE 1394 bus itself becomes the controller.

[0013] Challenges for proponents of IEEE 1394 have been not been so much at the lower layers of operation, that is in the physical, link and transaction layers (although bridges between protocols and data packet structure continue to be areas of contention), but rather in the high layers of the network protocol stack, such as the application layer. Recent developments in the broadcast television and cable industries, such as high definition television (HDTV) and consolidation in the cable broadcast industry are exponentially expanding the number of services and content available to consumers. To this end, interoperability between home electronic devices is strongly desired, as are common and/or standard functionality, ease of use and scalability. As such, there is a need for a system to control and manage the expanding array of devices and services that can be connected and supported, respectively, in a IEEE 1394-based home entertainment system.

SUMMARY OF THE INVENTION

[0014] In accordance with a first aspect of the present invention, a method is provided for address mapping in a network, such as, e.g., an IEEE 1394 based home entertainment network, which includes

receiving a self identification packet;
extracting a bus identifier and a physical identifier from the self identification packet;
adding a new row to an address mapping table, the new row comprising a bus identifier field, a physical identifier field, and a node unique identifier field;
inserting the physical identifier and bus identifier into the respective bus identifier and physical identifier field in the new row of the address mapping table;
transmitting a read request packet to a node identified by the self identification packet;
receiving a read response packet, the read response packet comprising a node unique identifier;
extracting one or more identifiers from the read response packet, the one or more identifiers including a node unique identifier; and
inserting the one or more identifiers into additional fields in the new row of the address mapping table.

[0015] As will be apparent to those skilled in the art, other and further aspects and advantages of the present invention will appear hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Preferred embodiments of the present invention are illustrated by way of example, and not by way or limita-

tion, in the figures of the accompanying drawings, in which like reference numerals refer to like components, and in which:

FIG. 1 depicts an exemplary IEEE 1394 module architecture;
FIG. 2 depicts a exemplary IEEE 1394 network topology;
FIG. 3 depicts an exemplary cable-based IEEE 1394 topology;
FIG. 4 depicts an exemplary IEEE 1394 node protocol stack;
FIG. 5 depicts a home gateway bridging multiple external service providers with a IEEE 1394-based network;
FIG. 6 is a functional block diagram of the home gateway of FIG. 5;
FIG. 7 is an alternate block diagram of the home gateway, illustrating hardware components;
FIG. 8 is block diagram illustrating a firmware stack for the home gateway;
FIG. 9 depicts a protocol stack for MPEG transport over the IEEE 1394-based home entertainment system network of FIG. 5;
FIG. 10 depicts a protocol stack for IP routing over the home entertainment system network of FIG. 5;
FIG. 11 depicts a protocol stack for IP plug-and-play and DNS/DHCP routing over the home entertainment system network of FIG. 5;
FIG. 12 depicts a protocol stack for bitmap display data transfer between devices of the home entertainment system of FIG 5;
FIG. 16 depicts an address mapping table; and
FIG. 22 is a flowchart depicting the acts for generating and maintaining an address mapping table.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] The IEEE 1394-1995 standard, which is hereby fully incorporated herein by reference for all that it describes and teaches, provides background information for the following description and figures in the accompanying drawings. In particular, selected portions of the IEEE 1394-1995 standard are described with reference to FIGS. 1 through 4.

IEEE 1394 OVERVIEW

[0018] FIG. 1 depicts an exemplary IEEE 1394 module 100, which comprises a plurality of addressable nodes 104. Each node 104 may comprise a processor unit 108 and an I/O unit 112 interconnected via a local bus 128. Alternatively, a node 104 may comprise a memory unit 116. Each node 104 connects in a IEEE 1394 carrier 120 via a respective bus connector 124.

[0019] FIG. 2 depicts exemplary IEEE 1394 physical network topology 200, which comprises two IEEE 1394 "backplane environments" 216 respectively bridged to a IEEE 1394 "cable environment" 212.

[0020] In a backplane environment 216 the physical topology is a multidrop bus 215. The physical media includes two, single ended conductors that run the length of the backplane and have connectors distributed thereon for connecting a plurality of IEEE 1394 nodes 104.

[0021] In a cable environment 212, the physical topology is a "noncyclic" network (meaning that closed loops are not supported) with finite branches and extent. Respective IEEE 1394 cables 220 connect together ports 208 on different nodes 104. Each port 208 typically comprises terminators, transceivers, and arbitration logic circuitry (not shown). The cables 220 and ports 208 function, in part, as cable repeaters, which repeat signals incident thereon to an adjacent node 104. This repeating feature allows nodes 104 in the cable environment 212 to simulate a single, logical bus. When two differing IEEE 1394 buses are connected together, e.g., in a backplane environment 216 or in a cable environment 212, a bridge 204 is used to convert communications between the different network environments.

[0022] In accordance with the IEEE 1394 standard, a sixty-four bit addressing scheme is employed by the IEEE 1394 network 200. The upper sixteen bits of each address represent the "node_ID". The most significant ten bits of the node_ID identify the particular logical bus or "bus_ID" (e.g., bus 215) in the overall IEEE 1394 network 200. Thus, up to one thousand twenty three buses can be employed in the IEEE 1394 network 200. The next most significant six bits of the node_ID represent a particular node's physical address or "physical_ID". Sixty-three independently addressable nodes (e.g., nodes 104) can reside on a particular IEEE 1394 bus (e.g., bus 215). Various portions of the remaining forty-eight bits of address space are allocated for specific resources, either to a particular bus, or a particular node.

[0023] FIG. 3 depicts an exemplary IEEE 1394 cable topology 300. In accordance with this configuration, a number of nodes 104 are "daisy-chained" together between ports 208 by respective IEEE 1394 cables 304. Each node 104 acts as a repeater, repeating signals between one port 208 to the next port so they can be transmitted over the cables 304 between the respective nodes 104.

[0024] FIG. 4 depicts a protocol stack 400 illustrating the relationships between the hardware and software components within an exemplary IEEE 1394 node 104. In particular, four layers are depicted in the protocol stack 400: trans-

action layer 404, link layer 408, physical layer 412, and serial bus management layer 416. Additional layers (not shown), such as an application layer, may also be included in the protocol stack 400.

[0025] In particular, the transaction layer 404 defines a complete request-response protocol to perform bus transactions to support read, write and lock operations. The transaction layer 404 also provides a path for isochronous management data to get to the serial bus management layer 416.

[0026] The link layer 408 provides for one-way data transfer with confirmation of request (i.e., an "acknowledged datagram") service to the transaction layer 404. More particularly, the link layer 408 provides addressing, data checking and data framing for packet transmission and reception, and also provides an isochronous data transfer service directly to the application. This includes generation of timing and synchronization signals (e.g., a "cycle signal").

[0027] The physical layer 412 translates logical symbols used by link layer 408 into electrical signals for output onto a IEEE 1394 cable. The physical layer 412 also provides an arbitration service to ensure that only one node at a time is sending data. In a preferred embodiment, the physical layer 412 provides data resynch and repeat service, as well as automatic bus initialization.

[0028] The serial bus management layer 416 provides bus management, isochronous resource management and node control. For example, in the cable environment 212 of FIG. 2, the serial bus management layer's 416 isochronous resource manager 420 grants the resources necessary for the respective nodes 104 to allocate and deallocate cooperatively the isochronous resources, channels and bandwidth necessary for efficient and orderly isochronous operations.

[0029] A bus manager 424 provides services, such as performance optimization, power and speed management and topology management to other nodes, 104 on the bus. Finally, a node controller 428 manages all control and status registers needed by the nodes 104 on the bus, and communicates with the physical layer 412, the link layer 408, the transaction layer 404 and one or more other application layers (not shown).

HOME ENTERTAINMENT AND HOME OFFICE SYSTEM

[0030] FIG. 5 depicts a home gateway 504 bridging multiple external service providers to a preferred home entertainment and home office system network, referred hereafter as "home entertainment system network" 500. The home entertainment system network 500 is connected by an IEEE 1394 bus 568, which is preferably configured in a cable environment (described above with reference to FIGS. 2-3). In particular, a series of daisy-chained, IEEE 1394 cables 502 interconnect between ports of various electronics components of the home entertainment system 500 to form the IEEE 1394 bus 568. For example, a TV 506, a stereo 512, a VCR 516 and a DVD 520 are connected in one chain 560. In another chain 564, a personal computer 524, a printer 528, and a digital camera 534 are connected.

[0031] Each of the respective chains 560 and 564 of electronic components are connected to the home gateway 504, which acts as a bridge between one or more external networks and the respective internal network chains 560 and 564, (i.e., as opposed to a bridge between two different bus environments). For example, the home gateway 504 is capable of receiving media feeds from a satellite 582 via a satellite receiver 540, a broadcast tower 586 via an antenna 544, as well as feeds from local land lines 592 (e.g. copper twisted pair, coaxial or fiber optic cable) via a coaxial cable receiver 548, fiber optic cable receiver 552, or telephone cable receiver 556, respectively. (Note: although the various receivers are shown outside of the home gateway 504, the actual receivers or receptacles can be contained within the home gateway 504 as well. They are shown outside of the home gateway 504 for illustration purposes only.)

[0032] The TV 508 preferably includes an internal television adapter that converts data from the IEEE 1394 bus 502 to NTSC (National Television Standards Committee) and/or ATSC (Advanced Television Systems Committee) video signals for presentation on the television screen. In an alternative preferred embodiment, the television adapter is an external device, which connects between the TV 508 and the IEEE 1394 cable 502. In either embodiment, the television adapter preferably includes an off-screen buffer, for image data not presently displayed, but to be displayed in the future, and an on-screen buffer, for image data presently displayed on the television screen. Furthermore, the television adapter can be incorporated into an auxiliary device connected to the television, such as a VCR, a DVD player, or a digital camera.

HOME GATEWAY

[0033] FIG. 6 depicts a functional block diagram for the home gateway 504, as well as for the components communicatively coupled to the home gateway 504.

[0034] The gateway 504 comprises one or more interfaces to communicate over an access network 644 through which respective services are provided. For example, services from an internet access provider ("IAP") or internet service provider ("ISP") 640, or from a video service provider ("VSP") 648 can be provided by connecting the respective home gateway interface, e.g., wireless interface "Terrestrial Broadcast I/F" 650, "Satellite I/F" 652, asynchronous digital subscriber line interface "ADSL I/F" 656, asynchronous transfer mode interface "ATM I/F" 660, or hybrid fiber coaxial

interface "HFC I/F" 664, to the access network 644 via an appropriate network link, (e.g., terrestrial link 618, satellite link 620, telephone link 624, fiber link 628 or coaxial link 632, respectively). According to one preferred embodiment, adapter slots on the home gateway 504 receive one or more of the above interfaces. Such an embodiment provides for a flexible reconfiguration when new or upgraded communications technologies/hardware are connected to the home entertainment system 500.

[0035] A variety of applications are possible over the access network 644 from either the IAP/ISP 640 and/or the VSP 648, such as internet surfing, MPEG video streams (standard and high definition television), network gaming, an electronic program guide "EPG", and home network control. Accordingly, the home gateway 504 includes hardware and software to enable home-user IP routing 668, MPEG2 stream handling (including on-screen display "OSD" and EPG processing) 672, access network communication control 676, home network control/management 630, and other resident or downloadable functions 682 such as gaming, home automation and directory services. To this end, the firmware stack for the home gateway 504 is described below with reference to FIG. 8. The protocol stacks for implementing the above referenced functions are described below with reference to FIGS. 9 through 12.

[0036] The 1394 interface 684 is a necessary component of the home gateway 504 and it is used in conjunction with the network protocols described with reference to FIGS. 9-12. The 1394 interface 684 acts as a bridge between the external network protocols and the IEEE 1394 compliant bus which forms the internal network. For example, the 1394 I/F 634 supports an IP over 1394 link 612 and an MPEG over 1394 link 616, between a personal computer 524 and a TV adapter 604 (which, in one embodiment, converts IEEE 1394 data into an analog or a digital signal for a television 608).

[0037] As illustrated in FIG. 7, one embodiment of the home gateway 504 includes a power supply circuit 748, a reset circuit 752, a clock circuit 756, a central processing unit "CPU" 704, a local bus 706, a PCI bridge & peripheral controller 708, non-volatile memory (e.g., ROM 712 and FLASH 716), volatile memory (e.g., DRAM 720), an RS232 interconnect, and a PCI bus 724. Connected to the PCI bus 724 are an ATM LSI interface 728, which provides an ATM bridge and other functionality to the home gateway 504, a synchronous optical network ("SONET") interface 732, which connects to an optical carrier 3 ("OC-3") level port, a 1394 LINK LSI 736, a 1394 PHY LSI, with three IEEE 1394 ports, and a register, LED and dip-switch unit 744.

[0038] Off-the-shelf hardware components are preferrably employed in the home gateway 504. For example, a presently preferred hardware component specification is set forth in Table 1. Where a particular manufacturer's product is preferred, it is specified.

Table 1

CPU	NR4650 133MHz (NKK Micro Devices)
DRAM	8 MB
ROM	128 kB
FLASH	4 MB
PCI Bridge & Peripheral Controller	NR4650-PSC (NKK Micro Devices)
1394 LINK LSI	MD8411 (Fuji Film Micro Device)
1394 PHY LSI	MD8401 (Fuji Film Micro Device)
ATM LSI	LASAR-155 (PMC-Sierra)
Internal Bus	PCI

[0039] The CPU 704, ROM 712, FLASH 716, RS232 724 and DRAM 720 are communicatively coupled to each other via PCI bridge & peripheral controller 708 and local bus 706. The PCI bridge & peripheral controller 708 is also connected to the PCI bus 724. The PCI bus 724 is, in turn, connected to the ATM LSI 728, the 1394 LINK LSI 736 and register, LED and dip-switch unit 744.

[0040] FIG. 8 depicts a firmware stack 800, employed by the home gateway 504. An operating system (OS) kernel 804 resides at the core of the firmware stack 800, and communicates with a service controller 808, system management 812, ATM driver 816 and 1394 driver 820. The ATM driver 816 communicates with the service controller 808, the 1394 driver 820 and various hardware components 824 (i.e., physical electronics components in the home entertainment system 500.). Similarly, the 1394 driver 820 communicates with the service controller 808, ATM driver 816 and hardware 824.

[0041] System management 812 includes functions for initialization, self-diagnostics, system health checking and

debugging. Service controller 808 includes functions for MPEG TS and EPG filtering and multicasting, IP routing and terminal functions, MPEG over the 1394 bus and MPEG over ATM, as well as IP over 1394 bus and IP over ATM, address mapping, home network service command and control (e.g., MPEG service control, TV image control, remote handling, and camera control), and other functions (e.g., gaming, home automation, and directory services)

[0042] The 1394 driver 820 realizes asynchronous data transmission, isochronous data transmission, physical layer control packet transmission, bus reset and control, root and cycle master processing, configuration status register and configuration ROM handling, bus management and address mapping table updates, whereas the ATM driver 816 realizes ATM pack transmission and ATM permanent virtual connection ("PVC") establishment and release.

[0043] The OS kernel 804 provides for task switching, message queue and delivery, interrupt handling, timer management and memory management. Also, the OS kernel 804 provides the electronic device interoperability functions which are used to control home gateway 504.

[0044] The hardware 824 represents the physical layer, or lowest layer, of the firmware stack 800.

PROTOCOL STACKS

[0045] FIGS. 9 through 12 depict various aspects of the protocol stacks employed between the respective external networks, the home gateway and the internal network(s), which pertain to the home entertainment system network. FIGS. 9-11 pertain to the home gateway 504. FIG. 12 pertains to the protocol stack between home electronic devices located on the home entertainment system network.

[0046] Commonly shown in FIGS. 9-12 is an external network 904, a bridge 908, and an internal network (i.e., IEEE 1394 bus) 912. The external network 904 can comprise an MPEG network 916 (e.g., a digital video service provider), and an IP network 920 (e.g., the "Internet"). An access network 924 connects to both the MPEG network 916 and IP network 920. According to one embodiment, the access network 924 is an Internet access provider ("IAP") such as, e.g., America Online or @Home. The external network 904 is coupled to the internal network 912 through a bridge 908. The bridge 908 is preferably an home gateway 504. The home gateway 504 converts data and signals from the external network 924 from ATM packets to an IEEE 1394 format, which can be forwarded to the internal network 912. The internal network 912 comprises a television adapter 932 and a standard or high definition television 936 (or alternatively a single unit incorporating a 1394 node and a television) and a personal computer 946. The protocol stacks are depicted in FIGS 9-12 under the portion of the overall system to which they correspond.

[0047] FIG. 9 depicts the protocol stack 900 according to ATM data transmission from an MPEG network 916 to a TV adapter 932.

[0048] MPEG data is formatted at the MPEG network 916 from MPEG TS ("transport stream") protocol or control command ("CTRL COM") 952 to ATM adaption layer 5 ("AAL5") 952. From AAL5, the data is converted to ATM data 948, and from ATM 948 it is converted to synchronous optical network "SONET" protocol 944. An ATM network is preferred at the lowest layer, given its high reliability, but in alternative embodiments, a different carrier can be employed (e.g., by replacing the ATM layers).

[0049] From the access network 924, data is received at the home gateway 504. At the home gateway 504, the communications from the external network are converted (or "bridged") from an ATM protocol to an IEEE 1394 protocol. Additional protocol layer conversions are shown in FIG. 9, including IEC 61883 964, which formats MPEG data for IEEE 1394 communication and is further described in International Electrotechnical Commission Standard 61883 entitled "Digital Interface for Consumer Audio/Visual Equipment" and which is publicly available from the IEC (www.iec.org). IEEE 1394 protocol 968, is described in the IEEE 1394-1995 standard.

[0050] From the gateway 908, data is sent via IEEE 1394 protocol to the internal network 912, where it is subsequently converted back into an MPEG transport stream for presentation playback on a video display unit. It is further possible with TV adapter 932 to convert the data to an analog signal cable of providing audio/visual data to a standard or high definition television set. Preferably, however, TV 936 is capable of supporting MPEG data.

[0051] FIG. 10 depicts a protocol stack 1000 according to IP data transmission from IP network 920 to PC 946. The transmission control protocol ("TCP") or user datagram protocol ("UDP") 1008, which are described in publicly available documents Internet RFC 793 and Internet RFC 768 respectively, are layered over internet protocol ("IP") 1004, which is described in Internet RFC 791. This facilitates transmission of packet data from an internet (e.g., the Internet or World-Wide Web). At the home gateway 504 and PC 946, an IP over 1394 protocol 1012, described in Internet Engineering Task Force ("IETF") document "IPv4 over IEEE 1394", by Peter Johansson and available at http://www.ietf.org is employed. The IETF document "Ipv4 over IEEE 1394" is incorporated herein by reference in its entirety. The protocol stack 1000 is especially advantageous for finding or exploring content on the World-Wide Web and Internet.

[0052] FIG. 11 illustrates a protocol stack 1100 for TCP/IP data transmission from the IP network 920 to the PC 946. In order to facilitate automatic setup and IP address assignments, the protocol stack 1100 supports a domain name system ("DNS"), as described in Internet RFCs 1034 and 1035, and dynamic host configuration protocol ("DHCP").

[0053] FIG. 12 illustrates a protocol stack 1200 for bitmap transfer between devices (e.g., from the home gateway 504 or PC 946 to the TV adapter 932) over the internal network 912. The protocol stack 1200 employs additional and previously non-described protocol "DD-Connect AsyBmp" 1204. The "bitmap transfer" protocol is described in U.S. application Ser. No. [Not Yet Assigned] (attorney docket no. 236/259), entitled "BITMAP TRANSFER", which has been incorporated herein by reference in its entirety. The "AP" protocol 1208 is simply the particular protocol used at the application layer (e.g., a display protocol or a mouse protocol).

ADDRESS MAPPING

[0054] FIG. 16 depicts an exemplary address mapping table 1600. The address mapping table 1600 preferably comprises at least four columns and as many rows as there are devices on the home entertainment network 500. The address mapping table 1600 is preferably partitioned into three distinct sections. The first section 1620 comprises IEEE 1394 service data, the second section 1624 comprises MPEG service data, and a third section 1628 comprises IP service data. Each section has its own "mini-table" for information, although the address mapping table 1600 is physically a single table.

[0055] In the IEEE 1394 section 1620 the first column is the node unique ID column 1604, the node unique ID is permanently encoded into the hardware or ROM of the node 104. The next group of columns are node attribute columns 1602. The node attribute columns include a common name column 1608, which identifies a particular node by a user selected/programmed name that is stored in the node, a node_ID column 1612, which contains a dynamically assigned 16-bit node_ID, a node type column 1616, and an IP address column 1618.

[0056] In the MPEG service section 1624, the first column is the ATM VPI/VCI column 1632, the next column is the MPEG information column 1636, the third column is the isochronous channel column 1640 and the last column is the node unique ID column 1604.

[0057] In the IP service section 1628, the first column is the ATM VPI/VCI column 1632, the next column is the IP address column 1618, the third column is the node_ID column 1612, and the last column is the node unique ID column 1604.

[0058] The address mapping table 1600 is created by the IEEE 1394 driver (e.g., IEEE 1394 driver 816 shown in FIG. 8) when a bus reset occurs. The IEEE 1394 driver receives a response from each node in the IEEE 1394 bus (e.g., IEEE 1394 bus 568 shown in FIG. 5) identifying the node's node unique ID and other information. Based on the information received from the node, the IEEE 1394 driver adds the node unique ID to the address mapping table 1600 and then queries the particular node for additional information (e.g., common name, node capabilities and IP address). The IEEE 1394 driver assigns a valve to node_ID column 1612 for the node.

[0059] FIG. 22 is a flowchart depicting the acts for generating and maintaining the address mapping table 1600. The acts are performed by a "managing node" residing on the home entertainment network system 500 and, more preferably, the acts are performed by the home gateway 504. The node managing the address mapping table 1600 is generally pre-selected. However, it can be dynamically changed either in response to a bus reset, or by express instruction from a user. In either event, the functionality for generating and maintaining the address mapping table 1600 is embedded into the IEEE 1394 driver 820.

[0060] At the outset of the address mapping process, a trigger is received which causes the address mapping table 1600 to be generated. The trigger is either an internal or external trigger, relative to the managing node, such as a bus reset command. The bus reset can occur as a result of an explicit instruction from the application layer, or by an implicit instruction from the firmware -- such as in response to the IEEE 1394 driver 820 detecting a new node added to the home entertainment network system 500. The trigger is shown as a bus reset in FIG. 22, act 2200.

[0061] After receiving a trigger, the processing continues to act 2204, where a self-identification packet is receiving by the managing node. The self-identification packet comprises sixteen-bit address information referred to above as a "node_ID". The node_ID, more particularly the ten-bit bus_ID and the six-bit physical_ID, is extracted from the self-identification packet at act 2208.

[0062] In act 2212, a new row is added to the address mapping table 1600. The data extracted at act 2208 is filled into the bus_ID and physical_ID fields in act 2216. In a preferred embodiment, the two fields are a single sixteen-bit address space -- i.e., the node_ID column 1612.

[0063] In act 2220, the managing node prepares and transmits an asynchronous read request addressed to the node identified by the node_ID received at act 2204. In response to the asynchronous read request, the managing node receives an asynchronous read response at act 2224. The asynchronous read response comprises at least a node unique identifier ("ID") and preferably also comprises additional node attribute information, such as an IP address, a node type, and a common name.

[0064] In act 2228, the node unique ID and, according to a presently preferred embodiment, the additional node attribute information, are extracted from the asynchronous read response received at act 2224. In act 2232, the node unique ID is filled into the node unique ID column of the address mapping table 1600. In a preferred embodiment, the

additional node attribute information is also filled into a corresponding column of the address mapping table 1600. In the event that a partitioned address mapping table 1600 is used, the rows of the address mapping table 1600 are logically separated corresponding to the type of service the data in the row pertains to, for example. IEEE 1394 service, ATM service, or MPEG service. In such an embodiment, the node attribute information identifies which partition the node information corresponds to. In another embodiment, redundant data is stored in mini service tables within the primary address mapping table 1600.

[0065] Finally, in act 2236, a test is performed to determine whether any new node self-ID packets have been received by the managing node. If any new node self-ID packets have been received, then processing continues to step 2208. If no new node self-ID packets have been received, then processing ends.

[0066] In the broader spirit of the invention, the steps described above can be handled in a batch mode, wherein after a bus reset (i.e., act 2200), a collection period elapses during which node self-ID packets are received and queued into a list in memory by the managing node. In such an embodiment, the processing of node self-IDs and the attainment of node unique IDs and node attribute information can be handled from the queued list in an incremental fashion. The test, therefore, in act 2236 becomes whether any additional self-ID packets need to be processed.

[0067] When a command directed toward a particular node in the home entertainment network system 500 is received, the command is related to the particular bus_ID and a physical_ID (or node_ID) using the address mapping table 1600. The managing node then uses the particular bus_ID and physical ID to address (or direct) the received command to a particular node in the home entertainment network system 500.

[0068] The methods and processes described herein are preferably performed by one or more processors executing one or more sequence of instructions stored on a computer-readable medium, such as a persistent disk, a CD-ROM, a floppy disk, a volatile memory (e.g., random access memory "RAM"), or a non-volatile memory (such as a flash memory or read-only memory "ROM"), rather than in a particular hardware arrangement. However, in the broader spirit of the inventions, various aspects of the methods and processes described herein can be implemented via hardware components such as TTL logic, or gate arrays. Furthermore, if a preference for a firmware level, e.g., a lower level programmic implementation of software component that is, generally, stored in ROM, or an application level, e.g., a higher level programmic implementation of a software component that runs over firmware, an operating system kernel, and/or server processes, software component is desired, then that preference is specified. If no preference is specified, then either level of implementation is acceptable. Accordingly, the written description and accompanying figures contained herein are to be regarded in an illustrative, rather than a restrictive sense.

Claims

1. A method for address mapping in a network system, comprising:

   receiving a self identification packet;
   extracting a bus identifier and a physical identifier from the self identification packet;
   adding a new row to an address mapping table, the new row comprising a bus identifier field, a physical identifier field, and a node unique identifier field;
   inserting the physical identifier and the bus identifier into the respective bus identifier field and physical identifier field in the new row of the address mapping table;
   transmitting a read request packet to a node identified by the self identification packet;
   receiving a read response packet, the read response packet comprising a node unique identifier;
   extracting one or more identifiers from the read response packet, the one or more identifiers including a node unique identifier; and
   inserting the one or more identifiers into additional fields in the new row of the address mapping table.

2. The method of claim 1, the read response packet further comprising node attribute information, the method further comprising adding the node attribute information to one or more fields in the new row of the address mapping table.

3. The method of claim 1, further comprising partitioning a plurality of unique records into three or more logically distinct sections, the three or more logically distinct sections including:

   an IEEE 1394 bus service section;
   an MPEG service section; and
   an IP service section.

4. The method of claim 1, further comprising:

receiving a command pertaining to a particular node in the network system;
relating the command to a particular bus identifier and physical identifier using the address mapping table; and
sending the command to the particular node using the particular bus identifier and physical identifier.

5. The method of claim 1, wherein the transmitting and receiving acts are performed via an IEEE 1394 bus.

6. The method of claim 1, wherein the network system comprises a home entertainment system.

7. A computer readable medium having stored thereon sequences of instructions for causing one or more processors to perform the acts of:

receiving a self identification packet;
extracting a bus identifier and a physical identifier from the self identification packet;
adding a new row to an address mapping table, the new row comprising a bus identifier field, a physical identifier field, and a node unique identifier field;
inserting the physical identifier and the bus identifier into the respective bus identifier field and physical identifier field in the new row of the address mapping table;
transmitting a read request packet to a node identified by the self identification packet;
receiving a read response packet, the read response packet comprising a node unique identifier;
extracting one or more identifiers from the read response packet, the one or more identifiers including a node unique identifier; and
inserting the one or more identifiers into additional fields in the new row of the address mapping table.

8. The computer readable medium of claim 7, further comprising sequences of instruction for causing the one or more processors to perform the act of partitioning a plurality of unique records into three or more logically distinct sections, the three or more logically distinct sections including:

an IEEE 1394 bus service section;
an MPEG service section; and
an IP service section.

9. The computer readable medium of claim 7, further comprising sequences of instruction for causing the one or more processors to perform the acts of:

receiving a command pertaining to a particular node in the network system;
relating the command to a particular bus identifier and physical identifier using the address mapping table; and
sending the command to the particular node using the particular bus identifier and physical identifier.

10. The computer readable medium of claim 7, wherein the sequences of instructions cause the one or more processors to perform the acts of transmitting and receiving via an IEEE 1394 bus.

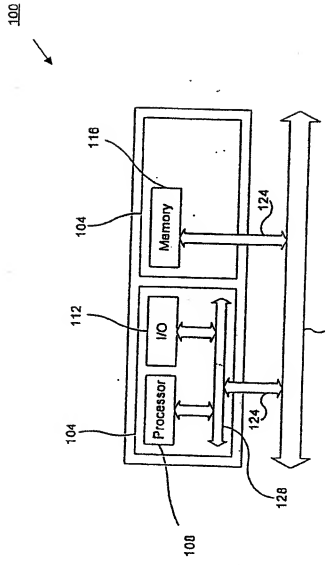

FIG. 1

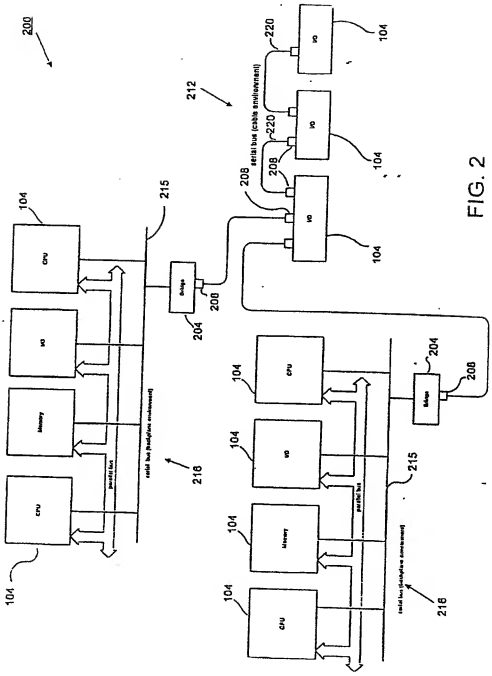
200
104
CPU
I/O
Memory
parallel bus
serial bus (duplex simplexed)
216
215
Bridge
204
206
208
212
serial bus (cable simplexed)
220
I/O
104
CPU
Memory
I/O
parallel bus
serial bus (duplex simplexed)
216
215
Bridge
204
208

FIG. 2

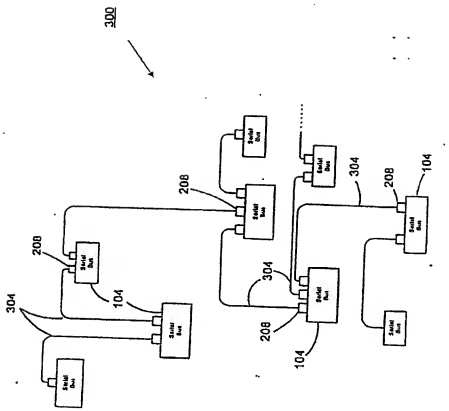

FIG. 3

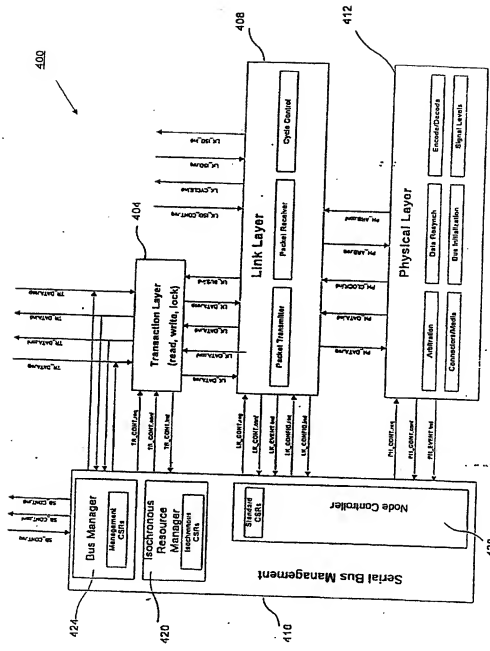
400
408
412
404
Link Layer
Cycle Control
Packet Receiver
Packet Transmitter
Physical Layer
Encode/Decode
Data Resynch
Bus Initialization
Arbitration
Connection Mode
Signal Levels
Transaction Layer
(read, write, lock)
Serial Bus Management
Node Controller
Isochronous
Resource
Manager
Bus Manager
Management
CSRs
Isochronous
CSRs
Standard
CSRs
424
420
410
428

FIG. 4

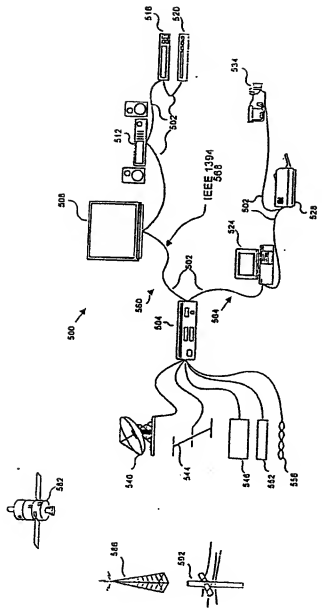
500
502
504
506
508
510
512
514
516
518
520
522
524
526
528
530
532
534
536
538
540
542
544
546
548
550
IEEE 1394
BUS

FIG. 5

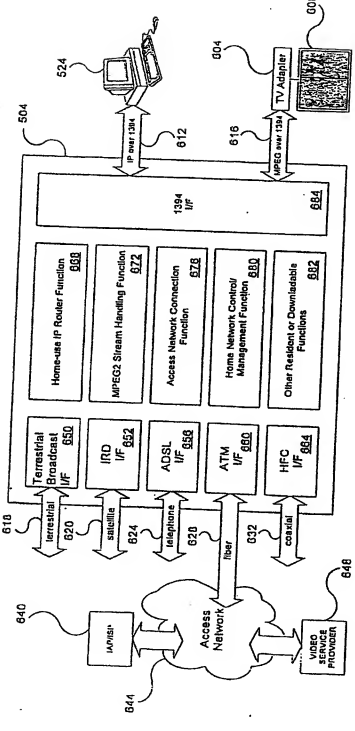
504
524
612
IP over 1394
004
008
TV Adapter
616
MPEG over 1394
1394 I/F
684
Home-use IP Router Function 668
MPEG2 Stream Handling Function 672
Access Network Connection Function 676
Home Network Control/ Management Function 680
Other Resident or Downloadable Functions 682
Terrestrial Broadcast I/F 650
IRD I/F 662
ADSL I/F 658
ATM I/F 660
HFC I/F 664
610
terrestrial 620
satellite 624
telephone 628
fiber
632
coaxial
648
640
IAP/ISP
641
Access Network
VIDEO SERVICE PROVIDER

FIG. 6

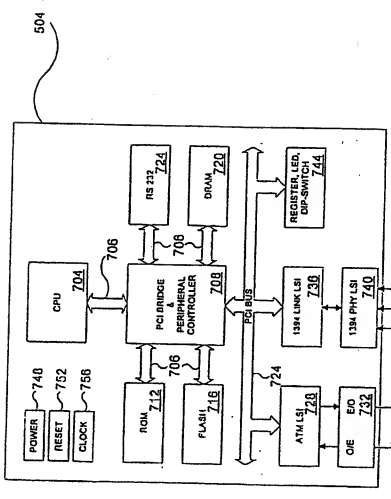
504
CPU
704
706
PCI BRIDGE
PERIPHERAL
CONTROLLER
708
706
706
706
RS 232
724
DRAM
720
REGISTER, LED,
DIP-SWITCH
744
PCI BUS
724
1394 LINK LSI
738
1394 PHY LSI
740
1394
POWER
740
RESET
752
CLOCK
756
ROM
712
FLASH
716
ATM LSI
728
EPD
732
OIE
OC-3

FIG. 7

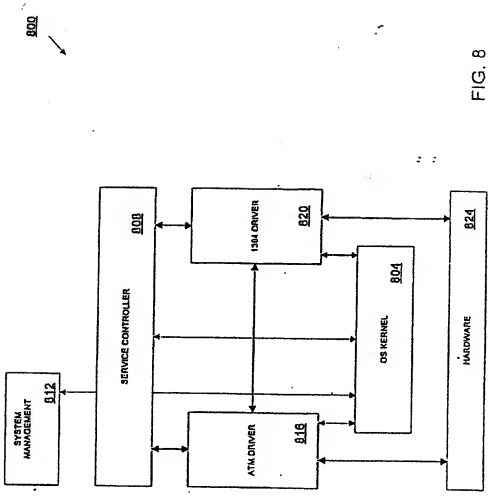
800
SYSTEM MANAGEMENT
812
SERVICE CONTROLLER
808
1394 DRIVER
820
OS KERNEL
804
ATM DRIVER
816
HARDWARE
824

FIG. 8

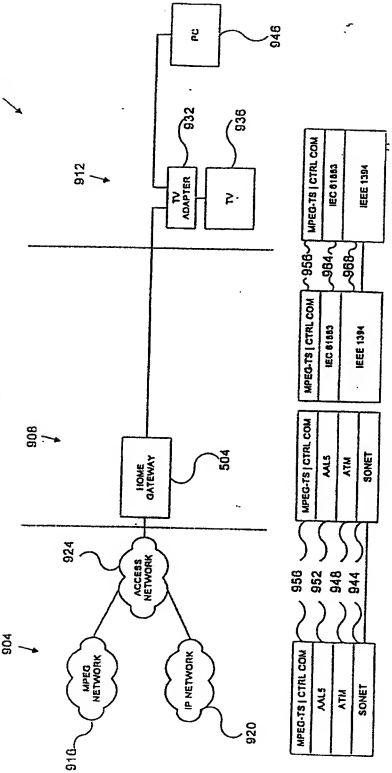
900
904
910
MPEG NETWORK
920
IP NETWORK
924
ACCESS NETWORK
908
HOME GATEWAY
504
912
TV ADAPTER
932
TV
936
PC
946
MPEG-TS | CTRL COM
AAL5
ATM
SONET
956
952
948
944
MPEG-TS | CTRL COM
AAL5
ATM
SONET
MPEG-TS | CTRL COM
IEC 61883
IEEE 1394
MPEG-TS | CTRL COM
IEC 61883
IEEE 1394
956
964
968

FIG. 9

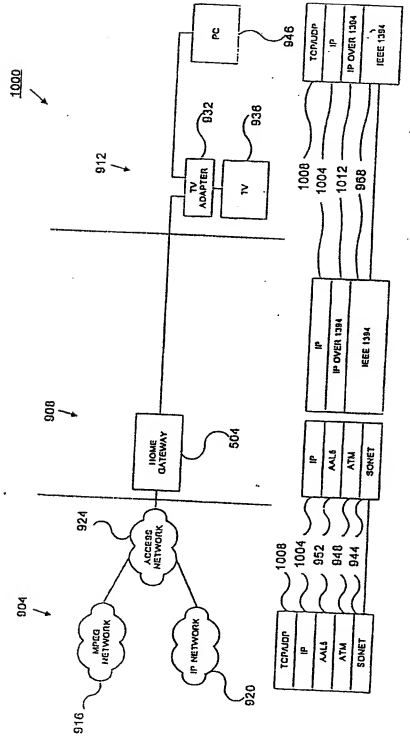
1000
904
916
MPEG NETWORK
920
IP NETWORK
924
ACCESS NETWORK
908
HOME GATEWAY
504
912
TV ADAPTER
932
TV
936
PC
946
1008
1004
952
948
944
TCP/UDP
IP
AAL5
ATM
SONET
1008
1004
1012
968
IP
IP OVER 1394
IEEE 1394
TCP/UDP
IP
IP OVER 1394
IEEE 1394

FIG. 10

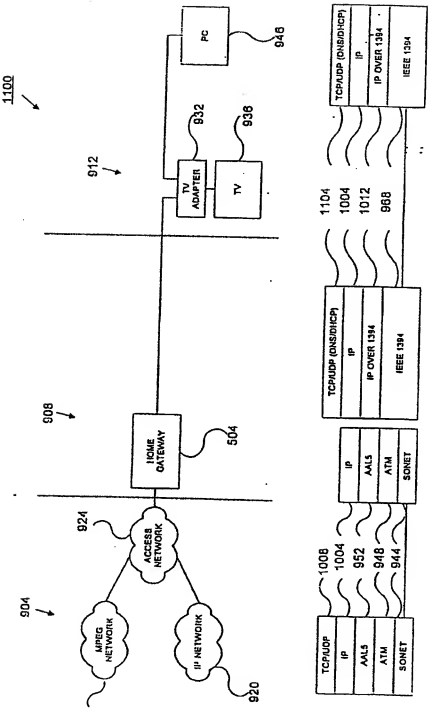
1100
904
916
MPEG NETWORK
924
ACCESS NETWORK
908
HOME GATEWAY
504
912
TV ADAPTER
932
TV
936
PC
946
920
IP NETWORK
TCP/UDP
IP
AAL5
ATM
SONET
1008
1004
952
948
944
IP
AAL5
ATM
SONET
1104
1004
1012
968
TCP/UDP (DNS/DHCP)
IP
IP OVER 1394
IEEE 1394
TCP/UDP (DNS/DHCP)
IP
IP OVER 1394
IEEE 1394

FIG. 11

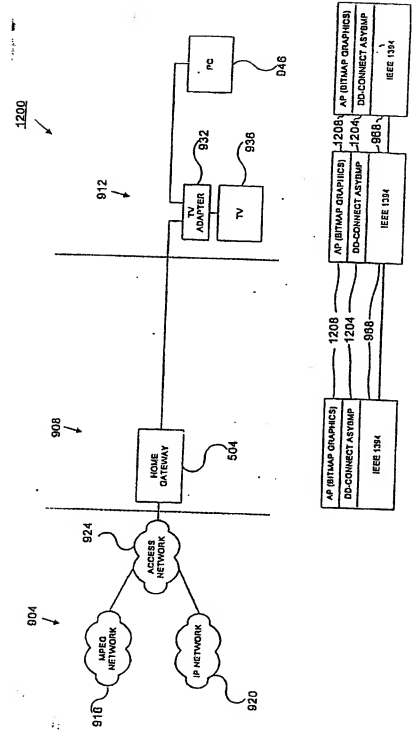
1200
912
PC
946
TV ADAPTER
932
TV
936
908
HOME GATEWAY
504
924
ACCESS NETWORK
904
MPEG NETWORK
910
IP NETWORK
920
AP (BITMAP GRAPHICS)
DD-CONNECT ASYNMP
IEEE 1394
1208
1204
988

FIG. 12

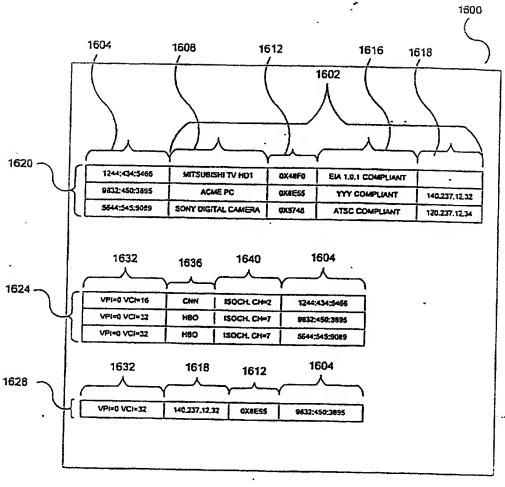
1600
1604
1608
1612
1616
1618
1602
1620
1244:434:5466
MITSUBISHI TV HD1
0X48F0
EIA 1.0.1 COMPLIANT
9832:450:3895
ACME PC
0X8E55
YYY COMPLIANT
140.237.12.32
5644:545:9089
SONY DIGITAL CAMERA
0X9748
ATSC COMPLIANT
120.237.12.34
1632
1636
1640
1604
1624
VPI=0 VCI=16
CNN
ISOCH. CH=2
1244:434:5466
VPI=0 VCI=32
HBO
ISOCH. CH=7
9832:450:3895
VPI=0 VCI=32
HBO
ISOCH. CH=7
5644:545:9089
1632
1618
1612
1604
1628
VPI=0 VCI=32
140.237.12.32
0X8E55
9832:450:3895

FIG. 16

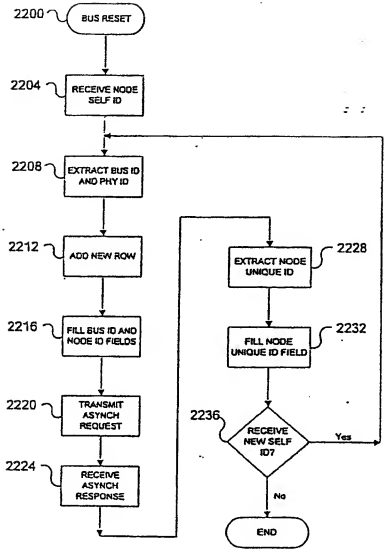
2200
BUS RESET
2204
RECEIVE NODE SELF ID
2208
EXTRACT BUS ID AND PHY ID
2212
ADD NEW ROW
2216
FILL BUS ID AND NODE ID FIELDS
2220
TRANSMIT ASYNCH REQUEST
2224
RECEIVE ASYNCH RESPONSE
2228
EXTRACT NODE UNIQUE ID
2232
FILL NODE UNIQUE ID FIELD
2236
RECEIVE NEW SELF ID?
Yes
No
END

FIG. 22

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 049 309 A3

(12) **EUROPEAN PATENT APPLICATION**

(88) Date of publication A3:
12.03.2003 Bulletin 2003/11

(43) Date of publication A2:
02.11.2000 Bulletin 2000/44

(21) Application number: **00108805.3**

(22) Date of filing: **26.04.2000**

(51) Int Cl.7: **H04L 29/12**, H04L 12/28

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **29.04.1999 US 304212**

(71) Applicant: **MITSUBISHI DENKI KABUSHIKI KAISHA**
Tokyo 100-8310 (JP)

(72) Inventors:
- **Akatsu, Shinji**
  2 chome, Chiyoda-Ku, Tokyo 100-8310 (JP)
- **Matsubara, Fernando-Masami**
  Apt: 201 Santa Carla, CA 95054 (US)
- **Miura, Shin**
  2-chome, Chiyoda-ku, Tokyo 100-8310 (JP)

(74) Representative: **Pfenning, Meinig & Partner**
Mozartstrasse 17
80336 München (DE)

(54) **Address mapping**

(57) A method for address mapping in a home entertainment network system includes receiving a self identification packet; extracting a bus identifier and a physical identifier from the self identification packet: adding a new row to an address mapping table, the new row comprising a bus identifier field, a physical identifier field, and a node unique identifier field; inserting the physical identifier and bus identifier into the respective bus identifier and physical identifier field in the new row of the address mapping table; transmitting a read request packet to a node identified by the self identification packet; receiving a read response packet, the read response packet comprising a node unique identifier; extracting one or more identifiers from the read response packet, the one or more identifiers including a node unique identifier; and inserting the one or more identifiers into additional fields in the new row of the address mapping table.

EP 1 049 309 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 10 8805

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X Y	US 5 764 930 A (STAATS ERIK P) 9 June 1998 (1998-06-09) * column 2, line 6 - line 24 * * column 4, line 45 - line 60 * * column 5, line 4 - line 27 * * column 5, line 47 - column 6, line 8 * * column 7, line 6 - line 16 * * column 8, line 35 - line 41 * * figures 1,2 * ---	1,4,5,7, 9,10 2,3,6,8	H04L29/12 H04L12/28
X,P	EP 0 932 275 A (SONY ELECTRONICS INC) 28 July 1999 (1999-07-28) * paragraph [0001] * * paragraphs [0051],[0052] * * paragraphs [0116]-[0119] * * paragraphs [0130],[0131] * * paragraph [0134] * * figures 11A,13,15A * ---	1,2,4-7, 9,10	
Y	EP 0 837 579 A (TOKYO SHIBAURA ELECTRIC CO) 22 April 1998 (1998-04-22) * column 1, line 7 - line 33 * * column 5, line 41 - line 47 * * column 20, line 5 - line 21 * * column 22, line 52 - column 23, line 9 * * figures 3,4,6 * ---	2,3,6,8	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H04L H04N G11B
A	"IEEE Standard for a High Performance Serial Bus" 1996 , THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC. , NEW YORK, USA XP002225609 ISBN: 1-55937-583-3 * page 37 - page 38 * * page 203 - page 249 * --- -/--	1-10	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	14 January 2003	Homan, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 10 8805

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	WICKELGREN I J: "THE FACTS ABOUT FIREWIRE" IEEE SPECTRUM, IEEE INC. NEW YORK, US, vol. 34, no. 4, 1 April 1997 (1997-04-01), pages 19-25, XP002051393 ISSN: 0018-9235 * the whole document *	1-10	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	14 January 2003	Homan, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 10 8805

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

14-01-2003

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5764930	A	09-06-1998	NONE		
EP 0932275	A	28-07-1999	US	6838625 A	14-03-2000
			EP	0932275 A2	28-07-1999
			JP	11275117 A	08-10-1999
EP 0837579	A	22-04-1998	JP	10126423 A	15-05-1998
			EP	0837579 A2	22-04-1998